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10EE56

Fifth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Linear IC's and Applications

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting at least TWO questions from each part.*
2. Use of resistor and capacitor standard values list are permitted.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. With a neat circuit diagram, explain design and the operation of a high input impedance capacitor coupled voltage follower. Obtain the expression for input impedance of the circuit. **(08 Marks)**

b. Briefly discuss the upper cut off frequency of an op-amp circuit and show how the cut-off frequency can be set for inverting amplifier. **(06 Marks)**

c. Design a capacitor coupled inverting amplifier to operate with +20V supply. The minimum input signal level is 50mV, the voltage gain is to be 68, the load resistance is 500Ω, and the lower cutoff frequency is to be 200Hz. Use 741 op-amp. **(06 Marks)**

2 a. Briefly explain:
i) Loop gain
ii) Loop phase shift
iii) Phase margin
iv) Unity gain bandwidth **(08 Marks)**

b. Explain the frequency compensation technique, using a phase lag network. **(06 Marks)**

c. Calculate the slew rate limited cutoff frequency, maximum peak value of the sinusoidal output voltage and cut off frequency limits rise time, slew rate limited rise time for 741 op-amp. Given: peak of sine wave output is to be 6V, $s = 0.5$ v/μs and circuit to operate at 800kHz. **(06 Marks)**

3 a. With a neat circuit diagram, explain design and the operation of a precision full wave rectifier. **(08 Marks)**

b. With a neat circuit diagram and wave form explain the working of sample and hold circuit. **(06 Marks)**

c. Using Bi-polar op-amp, design a precision clipping circuit to clip a 100kHz sine wave at the ±3V level. **(06 Marks)**

4 a. With a circuit diagram, explain the working of a capacitor coupled crossing detector and give the design steps. **(07 Marks)**

b. Using a bipolar op-amp with a ±18V supply, design an inverting Schmitt trigger circuit to have UTP = 1.5V and LTP = -3V. **(06 Marks)**

c. Design a monostable multivibrator circuit, to have an output pulse width of 1ms when trigged by a 2V, 100μs input pulse. Use a 741 op-amp with a ±12V supply. Assume $V_{R_2} = 0.5V$. **(07 Marks)**

PART – B

5 a. With a neat circuit diagram and waveforms, explain the operation of triangular / rectangular wave generator. **(08 Marks)**

b. Using a 741 op-amp with a supply of ±15V, design a phase shift oscillator to have an output frequency of 5.5kHz. Given: $A_V = 29$. **(06 Marks)**

c. With a neat circuit diagram and waveform, explain the operation of Wein bridge oscillator. **(06 Marks)**

6 a. Sketch the circuit of a second order high pass filter. Explain its operation and design procedure with frequency response curve. **(08 Marks)**

b. Design a narrow band pass filter and explain frequency response with neat circuit diagram. **(06 Marks)**

c. Design a wide band rejection filter using first order high pass and low pass filters having $F_L = 2kHz$ and $F_H = 400Hz$, respectively with pass band gain at 2. **(06 Marks)**

7 a. Explain the following performance parameters of a voltage regulator:

i) Line regulation.

ii) Load regulation.

iii) Ripple rejection. **(06 Marks)**

b. With a neat circuit diagram, explain the operation of a precision voltage regulator. **(06 Marks)**

c. With a schematic diagram, explain LM217 integrated circuit voltage regulator. Calculate the resistance of R_1 and R_2 for the LM217 regulator to produce an output voltage of 9 volts. **(08 Marks)**

8 a. Explain with the block diagram, universal active filter. How can it be realized as a second order low pass, high pass and band pass filter? List the salient features of FTF-U2 specialized I_C filter. **(10 Marks)**

b. With a block diagram, explain the operation of phase locked loop. List out any four applications of phased locked loop principle. **(10 Marks)**

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